Exhibit 11

Exhibit 2 – Cray T3D

'156 Patent

Claim Limitation (Claim 7)	Exemplary Disclosure
[**156a**] A device comprising:	Cray T3D discloses a device. *See, e.g.*: "Cray Research is implementing a three-phase massively parallel processor (MPP) program. Our goal is to reach a sustained performance on real customer code of one trillion floating-point operations per second. This manual describes the basic architecture of the first-phase MPP system, the CRAY T3D system. The CRAY T3D system contains hundreds or thousands of microprocessors, each accompanied by a local memory. The system is designed to support different styles of MPP programming, such as data parallel, work-sharing, and message passing. The CRAY T3D system connects to a host computer system. The host system provides support for applications running on the CRAY T3D system. All applications written for the CRAY T3D system are compiled on the host system but run on the CRAY T3D system. The host system may be any Cray Research computer system that has an input/output subsystem model E (IOS-E). Host systems include the CRAY Y-MP E series computer systems, the CRAY Y-MP M90 series computer systems, and the CRAY C90 series computer systems. The host system may reside in the same cabinet as the CRAYT3D system. This configuration is called a single-cabinet configuration. The host system may also reside in a separate cabinet that is cabled to the CRAY T3D system cabinet. This configuration is called a multiple-cabinet configuration." CRAY T3D System Architecture Overview at 1-1.
[**156b**] at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first	Cray T3D discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See, e.g.*: "An MPP computer system contains hundreds or thousands of microprocessors, each

Exhibit 2 – Cray T3D

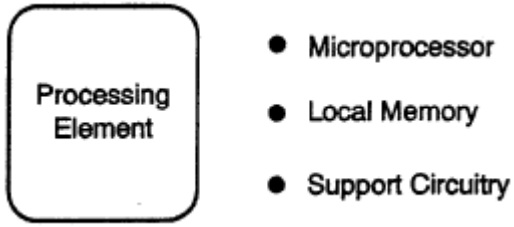
Claim Limitation (Claim 7)	Exemplary Disclosure
numerical value to produce a first output signal representing a second numerical value,	accompanied by a local memory. Each microprocessor and local memory component is called a processing element (PE). In the CRAY T3D system, each PE contains a microprocessor, local memory, and support circuitry (refer to Figure 1-2). There are two PEs per processing element node." CRAY T3D System Architecture Overview at 1-3.  "The microprocessor is a reduced instruction set computer (RISC) 64-bit microprocessor developed by Digital Equipment Corporation. The microprocessor performs arithmetic and logical operations on 64-bit integer and 64-bit floating-point registers [operations include the Institute of Electrical and Electronic Engineers (IEEE) floating point arithmetic]." CRAY T3D System Architecture Overview at 1-3. "Each processing element node contains two PEs, a network interface, and a block transfer engine (refer to Figure 1-3). The following paragraphs briefly describe each of these components.

Exhibit 2 – Cray T3D

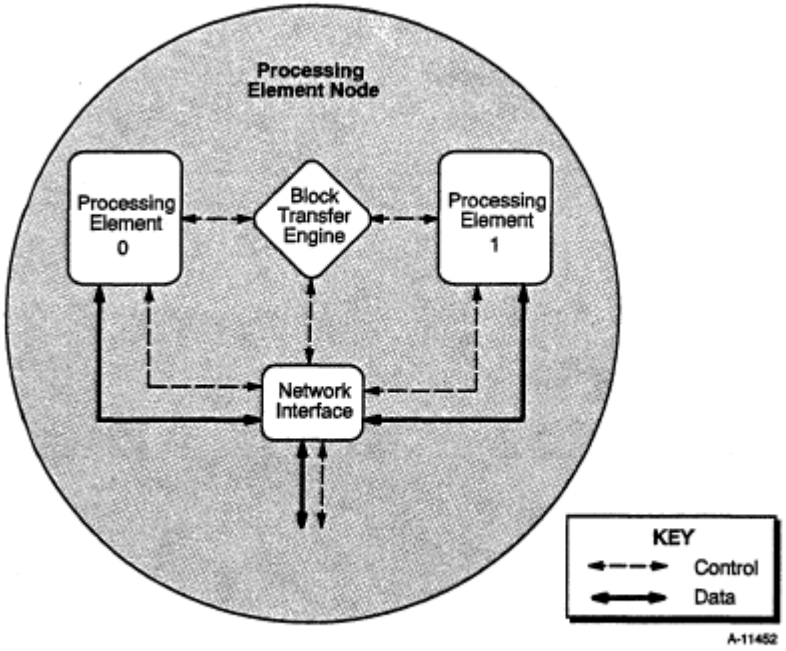
Claim Limitation (Claim 7)	Exemplary Disclosure
	 Figure 1-3. Processing Element Node The two PEs in a processing element node are identical but function independently. Access to the block transfer engine and network interface is shared by the two PEs. The network interface formats information before it is sent over the interconnect network to another processing element node or I/O gateway. The network interface also receives incoming information from another processing element node or I/O gateway and steers the information to PE 0 or PE 1 in the processing element node. The block transfer engine (BLT) is an asynchronous direct memory access controller that redistributes system data. The BLT redistributes system data between the local memory in PE 0 or

Exhibit 2 – Cray T3D

Claim Limitation (Claim 7)	Exemplary Disclosure
	PE 1 and globally addressable system memory. The BLT can redistribute up to 65,536 64-bit words of data (or 65,536 4-word lines of data) without interruption from the PE." CRAY T3D System Architecture Overview at 1-4 & Fig. 1-3. "I/O gateways transfer system data and control information between the host system and the CRAY T3D system or between the CRAY T3D system and an input/output cluster (IOC). The I/O gateways connect to the interconnect network through network routers that have communication links in the X and Z dimensions only. [The I/O gateways do not have connections in the Y dimension because the Y dimension connectors on an I/O gateway circuit board were replaced with low-speed (LOSP) and high-speed (HISP) channel connectors.] An I/O gateway can transfer information to any PE in the interconnect network.

Exhibit 2 – Cray T3D

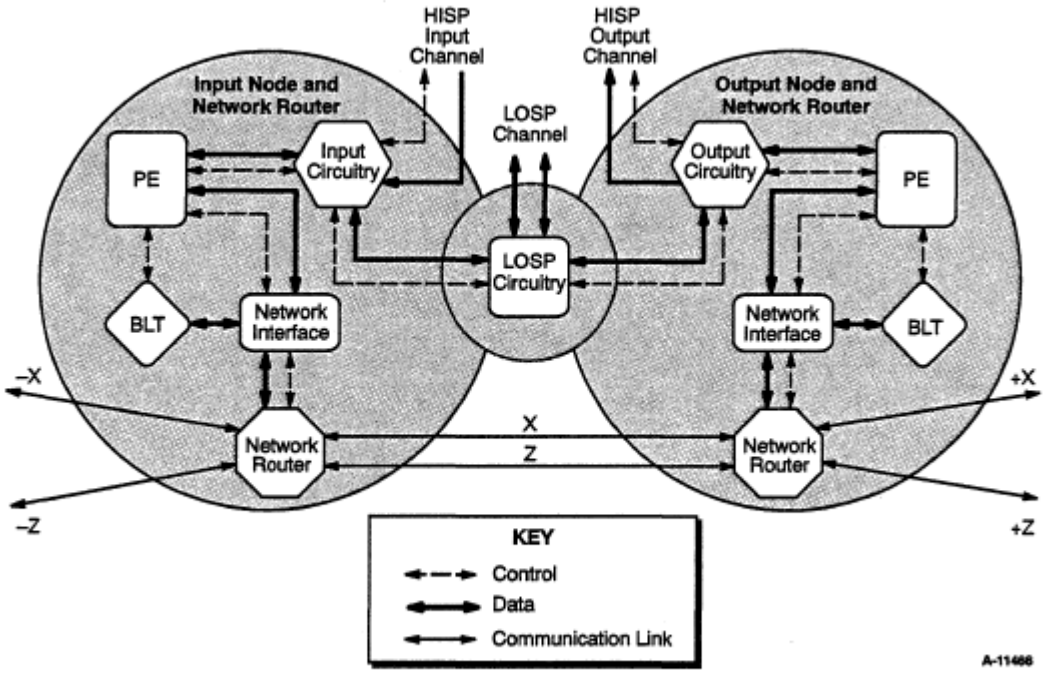
Claim Limitation (Claim 7)	Exemplary Disclosure
	 Figure 1-5. I/O Gateway The PE in the input node is designed to interface with the HISP input circuitry. Because of this characteristic, the PE in the input node does not contain the circuitry to perform all of the operations that a PE in a processing element node performs. Instead, the circuitry is replaced with circuitry that interfaces with the HISP input circuitry. In addition, half of the local memory in the PE is replaced with HISP input circuitry that contains HISP channel buffers. The HISP input circuitry receives incoming system data from the host system over the HISP channel. After receiving the data, the HISP input circuitry, PE, and BLT in the input node transfer the data to PEs in the CRAY T3D system.

Exhibit 2 – Cray T3D

Claim Limitation (Claim 7)	Exemplary Disclosure
	Except for HISP output circuitry replacing the HISP input circuitry, the output node is identical to the input node. The HISP output circuitry transmits outgoing system data to the host system over the HISP channel. After the PE and BLT in the output node retrieve data from PEs in the CRAY T3D system, the HISP output circuitry transfers the data to the host system. The LOSP circuitry transfers request and response information over the LOSP channel that connects the host system and the CRAY T3D system. LOSP request and response information is used to control the transfer of system data over the HISP channel. There are two types of I/O gateways: a master I/O gateway and a slave I/O gateway. The two types of I/O gateway correspond to the two types of components connected by a HISP channel. The master I/O gateway is the master component of a HISP channel and sends the address information to the host system during a HISP transfer. The slave I/O gateway is the slave component of a HISP channel and receives the address information from the host system during a HISP transfer." CRAY T3D System Architecture Overview at 1-6 through 1-5 & Fig. 1-5. As it relates to the Court's construction of LPHDR execution unit, Cray T3D included both addressable memory paired with the processing element(s) and control for the processing elements (to the extent that control is interpreted to include any signaling that affects the operation of the processing element). *See e.g.*, Cray T3D System Architecture Overview, at 3-10–3-17. For example, in the Cray-T3D, "[e]ach PE contains a microprocessor, local memory, and support circuitry." *Id.* at 3-10. The "support circuitry extends the control and addressing functions of the microprocessor." *Id.*, 3-17. Additionally, the microprocessor in each PE includes a "central control unit." *Id.*, at 3-12. To the extent Singular contends that the Cray-T3D did not include addressable memory paired with the processing element(s) and control for the processing elements, processing elements that were paired with addressable memory and control for the processing elements (to the extent that control is interpreted to include any signaling that affects the operation of the processing element) were well-known in the art, as explained in Section IV.C.1.d of the Amended Responsive Contentions Regarding Non-Infringement and Invalidity. *See*, *e.g.*, '273 patent, 3:49-56

Exhibit 2 – Cray T3D

Claim Limitation (Claim 7)	Exemplary Disclosure
	(describing admitted prior art). To the extent Singular nonetheless contends that one of skill in the art would have needed a motivation to combine Cray with processing elements with paired addressable memory and/or processing elements with control, one of skill in the art would have been motivated to do so based on the teachings of any of Dockser, Belanović, Belanović and Leeser, Shirazi, Lienhart, the admitted prior art, Patterson & Hennessy, in Computer Organization & Design, The Hardware Software Interface (3d. Ed. 2005), and/or Hamada.
[**156c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	Cray T3D discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. Specifically, the Cray T3D used number formats having an 11-bit exponent (from the IEEE double-precision floating-point format) but allowed the use of fewer precision bits by truncating the fraction down to 5-bits or more, which meets the claimed minimum error rate. *See, e.g.*: "The microprocessor is a reduced instruction set computer (RISC) 64-bit microprocessor developed by Digital Equipment Corporation. The microprocessor performs arithmetic and logical operations on 64-bit integer and 64-bit floating-point registers [operations include the Institute of Electrical and Electronic Engineers (IEEE) floating point arithmetic]." CRAY T3D System Architecture Overview at 1-3. "The floating-point execution unit performs floating-point operations on 64-bit floating-point registers. The floating-point operations include IEEE arithmetic instructions, plus instructions for performing conversions between floating-point and integer quantities. There are 32 floating-point registers." CRAY T3D System Architecture Overview at 3-13. "The -t *num* option specifies the number of bits to be truncated on floating-point operations. For *num*, enter an integer in the range of $0 \leq num \leq 47$. The default is 0." CF90™ Commands and

Exhibit 2 – Cray T3D

Claim Limitation (Claim 7)	Exemplary Disclosure
	Directives Reference Manual at 54. To the extent that Singular contends that Cray T3D does not disclose this limitation, notwithstanding its disclosure of a floating point format with 11 exponent bits and fraction bits capable of truncation down to 5-bits or more, that format would have been obvious to one of skill in the art for the reasons explained in the Responsive Contentions Regarding Non-Infringement and Invalidity ("Responsive Contentions"). Among other things, the Responsive Contentions explain how those skilled in the art could use reduced-precision formats depending on application specific needs. Specifically, the Responsive Contentions explain that the reduced-precision formats disclosed in any of Dockser, Lee, Belanović, Belanović and Leeser, Sudha, Shirazi, Aty, Xilinx, and TMS320C32 would have motivated one of skill in the art to use the functionality of the CrayT3D system to reduce the precision of the inputs to between 5 and 9 fraction bits. *See also* Appendix to Responsive Contentions (detailing error rates associated with different mantissa sizes).
[**156d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;	Cray T3D discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See, e.g.*: "The CRAY T3D system connects to a host computer system. The host system provides support for applications running on the CRAY T3D system. All applications written for the CRAY T3D system are compiled on the host system but run on the CRAY T3D system. The host system may be any Cray Research computer system that has an input/output subsystem model E (1OS-E). Host systems include the CRAY Y-MP E series computer systems, the CRAY Y-MP M90 series computer systems, and the CRAY C90 series computer systems. The host system may reside in the same cabinet as the CRAYT3D system. This configuration is called a single-cabinet configuration. The host system may also reside in a separate cabinet that is cabled to the CRAY T3D system cabinet. This configuration is called a multiple-cabinet configuration." CRAY T3D System Architecture Overview at 1-1. "**Phase 1 Configuration**

Exhibit 2 – Cray T3D

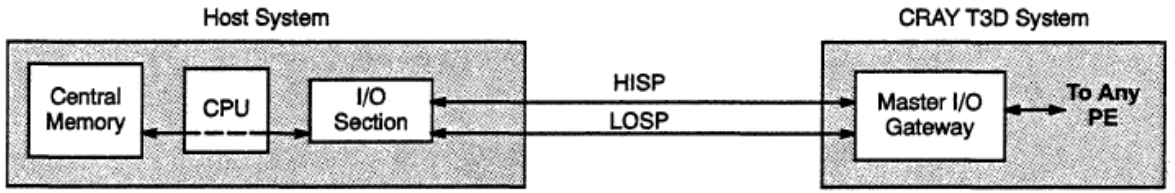
Claim Limitation (Claim 7)	Exemplary Disclosure
	Phase 1, which is provided with initial CRAY T3D systems, connects a master I/O gateway to the host system over the HISP channel. All configurations of the CRAY T3D system must have at least one phase 1 channel configuration (at least one master I/O gateway). The HISP and LOSP channels from the master I/O gateway connect to the circuitry on a CPU module or shared I/O module in the host system. Figure 4-5 shows the phase 1 channel configuration of a master I/O gateway.  Figure 4-5. Phase 1 I/O Gateway Channel Configuration When the CRAY T3D system connects to the host system through a master I/O gateway, the CPU in the host system controls all input and output. For example, the CPU controls tape, network, and disk device input and output. Data passes through the CPU and to the master I/O gateway." CRAY T3D System Architecture Overview at 4-5 & Fig. 4-5. "**Phase 2 Configuration** Phase 2, which will be available in the first half of 1994, connects a slave I/O gateway to an IOC that is also connected to a CPU. Figure 4-6 shows the phase 2 channel configuration of a slave I/O gateway.

Exhibit 2 – Cray T3D

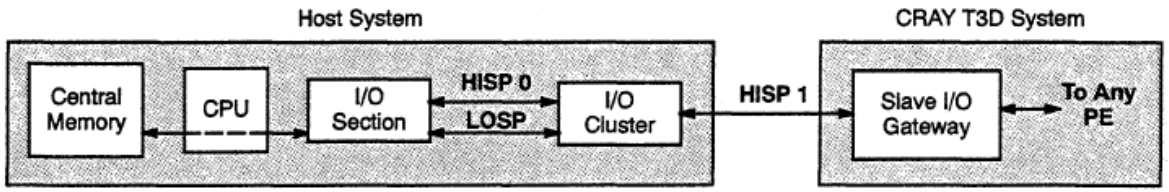
Claim Limitation (Claim 7)	Exemplary Disclosure
	 Figure 4-6. Phase 2 Slave I/O Gateway Channel Configuration When the CRAY T3D system connects to the host system using the phase 2 channel configuration, the CPU in the host system controls all input and output. For example, the CPU controls tape, network, and disk device I/O. Although the CPU controls the input and output, a HISP data path connects the CRAY T3D system to the IOC. This provides a path for data to travel between the CRAY T3D system and disk devices without traveling through the circuitry on a CPU module. The phase 2 configuration uses the back-door HISP software support that is also used for the SSD solid state storage device model E (SSD-E). If the slave I/O gateway is connected to an IOC in this configuration, the SSD-E in the host system cannot be configured with back-door capability to the same IOC." CRAY T3D System Architecture Overview at 4-6 & Fig. 4-6.
[**156e**] wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine;	Cray T3D discloses at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine. Specifically, Cray T3D discloses a "Host System" that included a CPU (or at least a state machine). *See, e.g.*: "**Phase 1 Configuration** Phase 1, which is provided with initial CRAY T3D systems, connects a master I/O gateway to the host system over the HISP channel. All configurations of the CRAY T3D system must have at least one phase 1 channel configuration (at least one master I/O gateway).

Exhibit 2 – Cray T3D

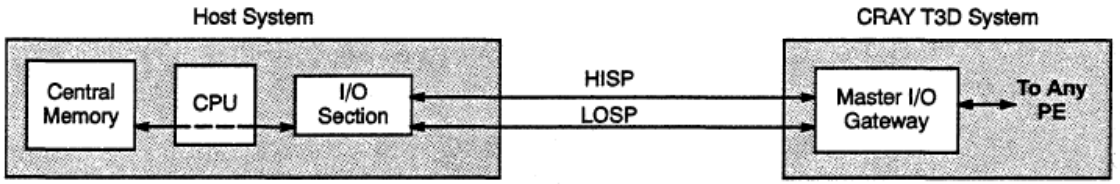
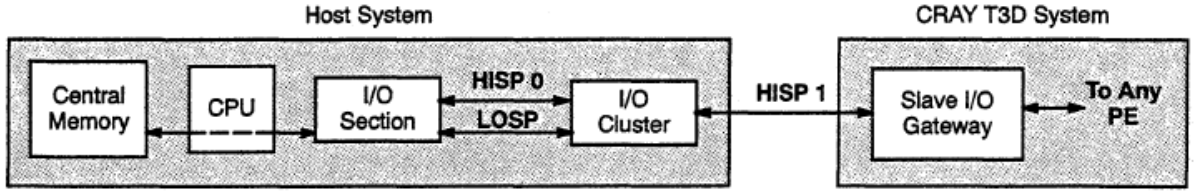
Claim Limitation (Claim 7)	Exemplary Disclosure
	The HISP and LOSP channels from the master I/O gateway connect to the circuitry on a CPU module or shared I/O module in the host system. Figure 4-5 shows the phase 1 channel configuration of a master I/O gateway.  Figure 4-5. Phase 1 I/O Gateway Channel Configuration When the CRAY T3D system connects to the host system through a master I/O gateway, the CPU in the host system controls all input and output. For example, the CPU controls tape, network, and disk device input and output. Data passes through the CPU and to the master I/O gateway." CRAY T3D System Architecture Overview at 4-5 & Fig. 4-5. "**Phase 2 Configuration** Phase 2, which will be available in the first half of 1994, connects a slave I/O gateway to an IOC that is also connected to a CPU. Figure 4-6 shows the phase 2 channel configuration of a slave I/O gateway.  Figure 4-6. Phase 2 Slave I/O Gateway Channel Configuration

Exhibit 2 – Cray T3D

Claim Limitation (Claim 7)	Exemplary Disclosure
	When the CRAY T3D system connects to the host system using the phase 2 channel configuration, the CPU in the host system controls all input and output. For example, the CPU controls tape, network, and disk device I/O. Although the CPU controls the input and output, a HISP data path connects the CRAY T3D system to the IOC. This provides a path for data to travel between the CRAY T3D system and disk devices without traveling through the circuitry on a CPU module. The phase 2 configuration uses the back-door HISP software support that is also used for the SSD solid state storage device model E (SSD-E). If the slave I/O gateway is connected to an IOC in this configuration, the SSD-E in the host system cannot be configured with back-door capability to the same IOC." CRAY T3D System Architecture Overview at 4-6 & Fig. 4-6.
[**156f**] and, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Cray T3D discloses the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See, e.g.*: "A CRAY T3D system contains 32; 64; 128; 256; 512; 1,024; or 2,048 PEs, depending on the system configuration (excluding the PEs in the I/O gateways). The PEs reside in processing element nodes." CRAY T3D System Architecture Overview at 1-3.

Exhibit 2 – Cray T3D

'273 Patent

Claim Limitation (Claim 53)	Exemplary Disclosure
[**273a**] A device:	Cray T3D discloses a device. *See* [**156a**].
[**273b**] comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Cray T3D discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**273c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	Cray T3D discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]. To the extent Singular contends that Cray T3D does not disclose this limitation, the limitation is obvious in light of Tong, Dockser, Lee, Belanović, Belanović and Leeser, Sudha, Shirazi, Aty, and TMS320C32. *See* [**156c**].
[**273d**] wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Cray T3D discloses the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See* [**156f**].

Exhibit 2 – Cray T3D

'961 Patent

Claim Limitation (Claim 4)	Exemplary Disclosure
[**961a**] A device comprising:	Cray T3D discloses a device. *See* [**156a**].
[**961b**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Cray T3D discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	Cray T3D discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]. To the extent Singular contends that Cray T3D does not disclose this limitation, the limitation is obvious in light of Tong, Dockser, Lee, Belanović, Belanović and Leeser, Sudha, Shirazi, Aty, and TMS320C32. *See* [**156c**].
[**961d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit.	Cray T3D discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See* [**156d**].

Exhibit 2 – Cray T3D

Claim Limitation (Claim 13)	Exemplary Disclosure
[**961e**] A device comprising:	Cray T3D discloses a device. *See* [**156a**].
[**961f**] a plurality of components comprising:	Cray T3D discloses a plurality of components. *See* [**156b**] + **[156d**].
[**961g**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Cray T3D discloses at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961h**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.	Cray T3D discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**]. To the extent Singular contends that Cray T3D does not disclose this limitation, the limitation is obvious in light of Tong, Dockser, Lee, Belanović, Belanović and Leeser, Sudha, Shirazi, Aty, and TMS320C32. *See* [**156c**].